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Question Paper Code : 80731

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2025.

Fifth/Sixth/Eighth Semester

Electronics and Communication Engineering

CEC 361 — VALIDATION AND TESTING TECHNOLOGY

(Common to : Electronics and Telecommunication Engineering)

(Regulations 2021)

Time : Three hours

Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. State the differences between MOS and CMOS technology.
2. Name two key applications of ion implantation in semiconductor manufacturing.
3. How does the figure of merit (ωo) affect the performance of MOS circuits?
4. Provide the relationship between I_{DS} and V_{DS} in a MOSFET.
5. Define latch-up in CMOS circuits.
6. Mention the advantages of using CMOS inverters over NMOS inverters.
7. State the impact of transistor sizing on the performance of CMOS circuits.
8. Define area capacitance units.
9. List the differences between observability and controllability in VLSI testing.
10. State the importance of testing in VLSI design and manufacturing.

PART B — (5 × 13 = 65 marks)

11. (a) Discuss the lithography process in detail. Explain how lithography impacts the feature size of transistors and its role in modern VLSI technology.

Or

- (b) Explain the importance of integrated resistors and capacitors in VLSI circuits. How are they fabricated, and what challenges are associated with their integration?

12. (a) (i) A MOSFET has a threshold voltage $V_{Th} = 0.6$ V. Calculate the drain current when $V_{GS} = 1.2$ V, $V_{DS} = 0.8$ V, and the transistor is in saturation. Assume $k' = 100 \mu A/V^2$ and $W/L = 10$. (7)
- (ii) Discuss how short channel effect occurs and its impact on the threshold voltage (V_{Th}) and device performance as the channel length is reduced. (6)

Or

- (b) Derive the I_{DS} - V_{DS} relationship for a nMOS transistor in both the linear and saturation regions. Explain how the transistor behaves in these regions.
13. (a) Given a CMOS inverter with threshold voltages $V_{Thn} = 0.4$ and $V_{Thp} = 0.4$ V, and power supply $V_{DD} = 5$ V, analyze its switching behavior, noise margins, and power dissipation.

Or

- (b) A nMOS inverter has a pull-up resistor of value $1 \text{ k}\Omega$ and the power supply voltage $V_{DD} = 5$ V. Calculate the logic threshold voltage (V_{Th}) and the power dissipation when the output is at logic "1" and "0". Compare it with the CMOS inverter in terms of efficiency.
14. (a) Derive the expression for sheet resistance in MOS circuits. How is it used in estimating resistance in a MOSFET's diffusion and polysilicon layers?

Or

- (b) A CMOS buffer is required to drive a capacitive load of 20 pF with a delay less than 5 ns . Calculate the necessary transistor sizing to meet the delay requirement (Risetime = fall time $\approx 1 \text{ ns}$).
15. (a) Explain the different fault models in VLSI testing. Illustrate with examples how fault models are used to improve fault coverage and ensure robust testing.

Or

- (b) A circuit has 1000 potential faults. After running a set of tests, 850 faults are detected. Calculate the fault coverage of the test. If the fault sampling rate is 80%, estimate how many faults would remain undetected, and discuss how improving test quality can increase fault coverage.

PART C — ($1 \times 15 = 15$ marks)

16. (a) (i) Discuss in detail the narrow channel width effect in MOS transistors. A MOS transistor has a width $W = 0.2 \mu\text{m}$. Mathematically explain how this narrow width affects the threshold voltage (V_{Th}) and the drive current of the transistor. (8)
- (ii) Explain the transconductance G_m and output conductance G_{Ds} of a MOS transistor. How do they influence the gain and bandwidth of an amplifier circuit? (7)

Or

- (b) Design a transmission gate using nMOS and pMOS transistors with threshold voltages $V_{Thn} = 0.5 \text{ V}$ and $V_{Thp} = -0.5 \text{ V}$. If the input signal varies from 0 to 5 V, calculate the on-resistance of the transmission gate at different input voltages. How does the transmission gate improve over a pass transistor for transmitting logic levels?

